REMARKS

A petition/fee letter for a one-month time extension is attached herewith.

The Examiner has reopened prosecution based on newly-cited US Patent Publication 2004/0173815 to Yeo et al., and newly-cited US Patent Publication 2005/0190421 to Chen et al. Applicants consider that, even in view of newly-cited Yeo and Chen, at least some dependent claims are allowable from the original claims. However, in an effort to expedite prosecution, Applicants have decided to attempt to amend the independent claims in view of these newly-cited references, rather than proceeding back up on Appeal at this time to get a final decision on which of the original dependent claims would be allowable in view of the newly-cited references.

Claims 1-4, 6, 10-15, and 23-30 are all the claims presently pending in the application. Claims 5, 7-9, and 16-22 are canceled.

It is noted that Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-4, 10, 11, 14, 15, and 23-30 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by newly-cited US Patent Publication 2004/0173815 to Yeo et al. Claims 1-4, 10, 11, 14, 15, and 23-30 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by newly-cited US Patent Publication 2005/0190421 to Chen et al.

Claims 1-15, and 23-30 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over previously-cited US Patent 6,909,151 to Hareland, further in view of one of previously-cited US Patent Publications: 2004/0227185 to Matsumoto et al., 2004/0075148 to Kumagai et al., or 2005/0079677 to Ke et al. Claims 5-9 and 13 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Yeo, further in view of Hareland. Claims 5-9 and 13 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Chen, further in view of Hareland.

Applicants traverse these rejections in the discussion that follows.

I. THE CLAIMED INVENTION

As described and defined in, for example, claim 1, the present invention is directed to a method of forming a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors. At least one localized stressor region is formed within the device, the at least one localized stressor region being located on one of the fin connectors.

Conventional methods, such as described in paragraphs [0005] through [0007], strain FinFETs by Si or SiGe, but have caused defects, thereby lowering yields.

The claimed invention, on the other hand, provides a localized stressor embedded within the device.

II. THE PRIOR ART REJECTIONS

The Rejections Based on Newly-Cited References Yeo and Chen

The Examiner alleges that newly-cited Yeo and newly-cited Chen anticipate the present invention described by independent claims 1 and 14. Applicants respectfully disagree.

These newly-cited references are specific to generating channel strain by implementing stress in the source-drain region for planar MOSFETs.

In contrast, the present invention is significantly different in that it applies stress in a novel way to a unique structure for the purpose of enhancing channel mobility.

That is, the present invention applies stress to FinFET devices in the region known as the Fin connector. In FinFET technology, typically more than one Fin is needed to create a single active device region for a FinFET device. The Fins comprising the active region for the device are connected by one of several techniques. One technique is to connect the Fins by using a lithography step during Fin patterning. Another technique for connecting the Fins is to merge Fins together after most of the front end of line processing is complete but before silicidation is performed.

Thus, in one exemplary embodiment, the present invention makes use of the Fin connector structures, which have absolutely no relation to the source/drain structures that Yeo or Chen uses, to create channel strain with localized stressors. In one exemplary embodiment, a

region of the Fin connector is silicided to create stress; in another exemplary embodiment, a hole is formed in the Fin connector such that the connection is not interrupted but a space is formed into which a stressed material may be deposited or grown.

In the rejection relative to original claims 5-9 and 13, the Examiner concedes that neither Yeo nor Chen teaches or suggests applying their stressors to Fin connector structures and relies upon secondary reference Hareland to overcome this deficiency. However, the rejection currently of record fails to demonstrate a localized stressor on a Fin connector in Hareland, and, therefore, fails to meet the initial burden of a *prima facie* rejection because it fails to demonstrate each element of the claimed invention.

Therefore, even if it were considered proper to combine Hareland with Yeo or Chen, the rejection would still be fundamentally deficient for failing to demonstrate the feature of incorporating a localized stressor to the Fin connector structures of a FinFET device, as required by the plain meaning of the claim language.

Hence, turning to the clear language of the claims, in neither Yeo nor Chen is there a teaching or suggestion of: "... forming at least one localized stressor region within said device, said at least one localized stressor region being located on one of said fin connectors", as required by independent claim 1. Independent claim 14 additionally requires that a localized stressor be formed on a second fin connector.

The Rejections Based on Previously-Cited Reference Hareland

The Examiner continues to allege that Hareland teaches the claimed invention defined in claims 1-15 and 23-30. Applicants again submit, however, that there are elements of the claimed invention which are neither taught nor suggested by Hareland.

Hareland discloses a FinFET device in which a film is deposited on top of the entire device that imparts stress in the channel of the device, thereby modifying the charge transport properties in the channel (mobility). The method in Hareland is almost identical to that taught in Assignee's patent US Patent Application 10/536,483, filed as a PCT Application on November 25, 2002, over a half year prior to Hareland's filing date.

In contrast to Hareland, the exemplary embodiment of the present invention provides an embedded stressor structure specifically in the fin connector part of the device (e.g., "localized ... within the device") that imparts stress in the channel of the FinFET. Dependent claims further

define that the localized stressors are located on specific structures within the device.

Hence, turning to the clear language of the claims, in Hareland there is no teaching or suggestion of: "... forming at least one localized stressor region within said device, said at least one localized stressor region being located on one of said fin connectors", as required by independent claim 1. Independent claim 11 has at least similar language.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Hareland. Therefore, the Examiner is respectfully requested to withdraw this rejection.

The Rejections Based on Newly-Cited Yeo/Chen, Further in View of Previously-cited Hareland

The Examiner rejects claims 5-9 and 13 as obvious over newly-cited Yeo and Chen, further in view of previously-cited Hareland. However, as pointed out above, Hareland fails to teach or suggest using localized stressors, let alone localized stressors on the Fin connector structures.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Hareland, and the Examiner is respectfully requested to withdraw these rejections.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-4, 6, 10-15, and 23-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

Date: 12/07/07

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